with a request from said data processor;

a first bus, having m (wherein m is an integer) bits width, connected between said memory and said memory controller, for transferring m bits of data in parallel; and

a second bus, having n (wherein n is an integer, n > m) bits width, connected between said memory controller and said data processor, for transferring n bits of data in parallel;

wherein said memory controller comprises:

a storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said first bus,

means for forming n bits of data using said successive groups of m bits of data and supplying said n bits of data in parallel to said data processor through said second bus based on an indicating from said data processor, and

a converter for converting said graphic data temporarily stored in said storage into serial data which is provided to said output means based on an indicating from said data processor.

49. (amended) A graphic processing apparatus comprising:

memory means for storing graphic data;

data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel,

wherein said memory controller includes:

storage means for temporarily storing graphic data read out from said memory means successively in a predetermined period of time via said first bus,

means for applying said temporarily stored graphic data to said data processing means as n-bit parallel data based on an indication from said data processing means, and

converting means for converting said temporarily stored graphic data into serial data and outputting the serial data to said output means based on an indication from said data processing means.

F2

F3

57. (amended) A graphic processing apparatus comprising:

memory means for storing graphic data, said memory means being accessed by using a row address and a column address;

data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel; and

wherein said memory controller includes:

means for reading out a plurality of graphic data at different column addresses at a same row address from said memory means via said first bus successively in a predetermined period of time,

means for applying said read-out graphic data to said data processing means as n-bit parallel data based on an indication from said data processing means, and

converting means for converting said read-out

graphic data into serial data and outputting the serial data to said output means based on an indication from said data processing means.

59. (amended) A memory controller for controlling transfer of data between memory means for storing graphic data and a processor and between said memory means and display means, comprising:

m-bit terminals (wherein m is an integer) connected to said memory means, for transferring data of m bits successively in a predetermined period of time between said memory means and said memory controller;

an n-bit interface (wherein n is an integer and n>m) connected to said processor, for transferring data of n bits in parallel between said processor and said memory controller based on an indication from said processor;

at least one bit terminal connected to said display means, for transferring serial data between said display means and said memory controller;

first converting means for performing conversion between data of plural sets of m bits via said m-bit terminals and data of n bits via said n-bit interface based on an indication from said processor; and

second converting means for converting said data of plural sets of m bits via said m-bit terminals into said serial data.

63. (amended) A memory controller for controlling

transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein successive groups of m bits of data is transferred through said m bit terminals between said memory and said controller by performing plural read operations within a memory cycle (where m is an integer);

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor (where n is an integer and n>m);

storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said m bit terminals;

means for forming n bits of data by combining successive groups of m bits of data from said m bit terminals and supplying said n bits of data in parallel to said n bit terminals based on an indication from said processor; and

converting means for converting said graphic data temporarily stored in said storage into serial data which is supplied to output means, said output means outputs graphic data read out from said memory based on an indication from said processor.

REMARKS

Claims 44-66 stand rejected as being based on a